CCSFP-S-LR-LC-1310-10-DDM

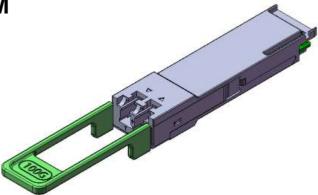## QSFP28 100G CWDM4 Transceiver

Features

- Hot Pluggable QSFP28 form factor
- Operating Data Rate up to 103.1Gb/s
- Duplex LC Connector Interface
- Up to 10Km over SMF
- 4x25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- 4x25G electrical interface
- Single 3.3V Power Supply
- Power dissipation <3.5W
- Operating case temperature range: 0°C to 70°C
- Compliant with SFF-8679
- Compliant with SFF-8636
- Compliant with CWDM4-MSA-Technical-Spec-1p1-1

Applications

- 100G CWDM4 applications with FEC

Part Number Ordering Information

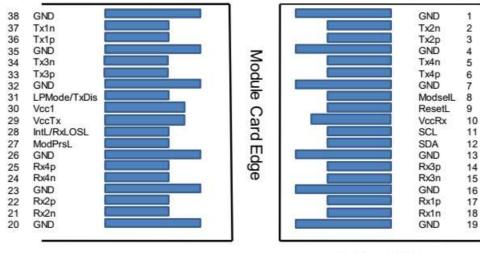| Part NO.	Data Rate	Fiber	Distance	Interface	Temp.
CCSFP-S-LR-LC-1310-10-DDM	103.1Gb/s	SMF	10Km	LC	Commercial

General Description

CCSFP-S-LR-LC-1310 QSFP28 transceiver module is designed for 103Gigabit Ethernet links over 10Km single mode fiber. It is compliant with CWDM4 MSA. Digital diagnostics functions are available via an I2C interface, as specified by the SFF-8636.

Electrical Connector

The following figure shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 38 pads intended for high speed signals,low speed signals, power and ground connections.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

       Connected first, disconnected last: - ground contacts
       Connected second, disconnected second: - power contacts
       Connected third, disconnected first: - signal contacts

38	GND
37	Tx1n
36	Tx1p
35	GND
34	Tx3n
33	Tx3p
32	GND
31	LPMode/TxDis
30	Vcc1
29	VccTx
28	IntL/RxLOSL
27	ModPrsL
26	GND
25	Rx4p
24	Rx4n
23	GND
22	Rx2p
21	Rx2n
20	GND

Top Side Viewed From Top

GND	1
Tx2n	2
Tx2p	3
GND	4
Tx4n	5
Tx4p	6
GND	7
ModselL	8
ResetL	9
VccRx	10
SCL	11
SDA	12
GND	13
Rx3p	14
Rx3n	15
GND	16
Rx1p	17
Rx1n	18
GND	19

Module Card Edge

Bottom Side Viewed From Bottom

Pin Description

Pad	Logic	Symbol	Description	Plug Seq.	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	Two-wire interface clock	3	
12	LVCMOS-I/O	SDA	Two-wire interface data	3	
13		GND	Ground	1	1

14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL /RxLOSL	Interrupt. Optionally configurable as RxLOSL via SFF-8636	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode /TxDis	Low Power Mode. Optionally configurable as TxDis via SFF-8636	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination.

Absolute Maximum Ratings

Exceeding any one of these values may damage the device permanently.

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	V_{CC}	-0.5		3.6	V
Storage Temperature	T_S	-40		+85	°C
Operating Relative Humidity	RH			85	%
Receiver Damage Threshold, per Lane	P_{Rdmg}	3.5			dBm

Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_{op}	0	25	+70	°C
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Power Dissipation	P_D			3.5	W

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data rata			$25.78125\pm100ppm$		Gbps	
Transmitter						
Differential data input swing	V_{in}			900	mVpp	
Input Impedance (Differential)	Z_{in}	90	100	100	ohm	
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter			IEEE 802.3bm Table 88-13			
Eye height		95			mV	
DC common mode voltage		-350		2850	mV	
Receiver						
Differential output amplitude		200		900	mVpp	
Output Impedance (Differential)	Z_{out}	90	100	110	ohm	
Output Rise/Fall Time	tr/tf	12			ps	20%~80%
Eye width		0.57			UI	
Eye height differential		228			mV	
Vertical eye closure				5.5	dB	

Optical Characteristics

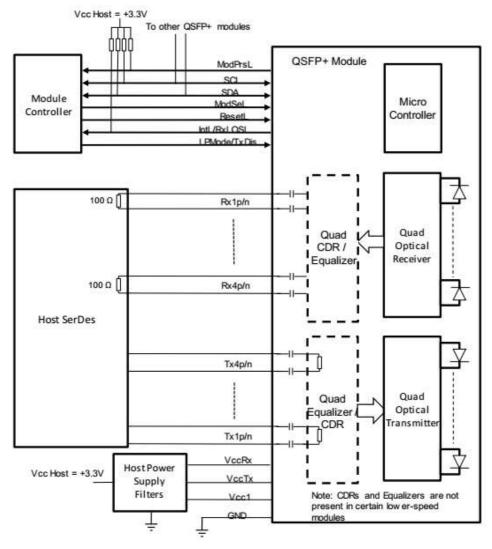| Parameter		Symbol	Min	Typ	Max	Unit	Note
Data rata			25.78125±100ppm			Gbps	
Center Wavelength	Lane1	λ_{C1}	1264.5	1271	1277.5	nm	
	Lane2	λ_{C2}	1284.5	1291	1297.5		
	Lane3	λ_{C3}	1304.5	1311	1317.5		
	Lane4	λ_{C4}	1324.5	1331	1337.5		
Transmitter							
Total Average Output Power		P_T			8.5	dBm	
Average Launch Power each Lane		AOP	-6.5		2.5	dBm	
Optical Modulation Amplitude each Lane		OMA	-4		2.5	dBm	
Extinction Ratio		ER	3.5			dB	
Transmitter and dispersion penalty, each lane		TDP			3	dB	
Launch power in OMA minus TDP, each lane				-5		dBm	
Side-mode Suppression ratio		SMSR	30			dB	
Optical return loss tolerance					20	dB	
Transmitter Reflectance		TR			-20	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2,Y3 }			{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				3
Receiver							
Average Receive Power each Lane		RXAOP	-13		2.5	dBm	
Receive Power (OMA) each Lane		RXOMA			2.5	dBm	
Receive Sensitivity in OMA each Lane at $5x10^{-5}$ BER		RXSEN			-11.5	dBm	
Stressed Receiver Sensitivity (OMA) each Lane		RXSRS			-9.1	dBm	4
Optical Return Loss		ORL			-26	dB	
LOS Assert		LOSA	-30			dBm	
LOS De-Assert		LOSD			-15	dBm	
LOS Hysteresis			0.5			dB	
Conditions of stressed receiver sensitivity test							
Vertical eye closure penalty		VECP		1.9		dB	
Stressed eye J2 Jitter		J2		0.33		UI	
Stressed eye J4 Jitter		J9		0.48		UI	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3}			{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				

Note 3: Hit ratio $5x10^{-5}$

Note 4: Measured with conformance test signal at TP3 for BER = $5x10^{-5}$

Recommend Circuit Schematic

Mechanical Specifications